What is Claimed is:

1. Apparatus for padding and transmitting initially unpadded blocks of data comprising:

means for deriving from a single reference clock signal first and second further clock signals having respective, different, first and second frequencies, the first frequency being suitable for use of the first further clock signal in at least some processing of the unpadded blocks, and the second frequency being suitable for use of the second further clock signal in at least some processing of the padded blocks.

2. The apparatus defined in claim 1 wherein the unpadded blocks are provided to the apparatus one after another at a predetermined rate, and wherein the apparatus further comprises:

means for transmitting the padded blocks one after another at the predetermined rate, each padded block being transmitted serially.

3. The apparatus defined in claim 2 further comprising:

means for accepting and registering each successive unpadded block.

4. The apparatus defined in claim 3 wherein the means for accepting and registering is at least partly controlled by the first further clock signal.

5. The apparatus defined in claim 4 further comprising:

means for adding padding to each unpadded block accepted and registered by the means for

accepting and registering to produce a corresponding padded block.

6. The apparatus defined in claim 1 further comprising:

means for serializing each padded block.

7. The apparatus defined in claim 6 wherein the means for serializing is at least partly controlled by the second further clock signal.

8. The apparatus defined in claim 5 further comprising:

means for serializing each padded block produced by the means for adding.

9. The apparatus defined in claim 8 wherein the means for serializing is at least partly controlled by the second further clock signal.

10. The apparatus defined in claim 1 wherein each unpadded block consists of 64 bits of data, and each padded block consists of 66 bits of data.

11. The apparatus defined in claim 1 wherein the means for deriving comprises:

first frequency dividing circuitry for dividing frequency of a common signal by a first division factor to produce the first further clock signal, the common signal coming from the reference clock signal.

12. The apparatus defined in claim 11 wherein the means for deriving further comprises:

second frequency dividing circuitry for dividing the frequency of the common signal by a second

division factor to produce the second further clock signal.

13. The apparatus defined in claim 11 wherein the means for deriving further comprises:

frequency multiplying circuitry for multiplying frequency of a signal coming from the reference clock signal to produce the common signal.

14. The apparatus defined in claim 13 wherein the means for deriving further comprises:

frequency pre-division circuitry for dividing frequency of the reference clock signal by a pre-division factor to produce the signal operated on by the frequency multiplying circuitry.

15. The apparatus defined in claim 2 wherein each unpadded block is supplied to the apparatus as a plural number of successive sub-blocks, each of which is supplied in parallel, the sub-blocks being supplied at a sub-block rate that is the predetermined rate times the plural number.

16. The apparatus defined in claim 2 wherein the reference clock signal has a reference frequency having an integer-based relationship to the predetermined rate.

17. The apparatus defined in claim 16 wherein the means for deriving comprises:

means for performing integer-based manipulation of the reference frequency to produce the first and second further clock signals.

18. The apparatus defined in claim 17 wherein the means for performing comprises:

first means for performing first integer-based manipulation of the reference frequency to produce a common signal; and

second means for performing second integer-based frequency manipulation of the common signal to produce the first further clock signal.

19. The apparatus defined in claim 18 wherein the means for performing further comprises:

third means for performing third integer-based frequency manipulation of the common signal to produce the second further clock signal.

20. A programmable logic device including apparatus as defined in claim 1.

21. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 20 coupled to the processing circuitry and the memory.

22. A printed circuit board on which is mounted a programmable logic device as defined in claim 20.

23. The printed circuit board defined in claim 22 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

24. The printed circuit board defined in claim 22 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

25. Apparatus for receiving and unpadding padded blocks of data comprising:

means for deriving from a single reference clock signal first and second further clock signals having respective, different, first and second frequencies, the first frequency being suitable for use of the first further clock signal in at least some processing of the padded blocks, and the second frequency being suitable for use of the second further clock signal in at least some processing of the unpadded blocks.

26. The apparatus defined in claim 25 wherein the padded blocks are received by the apparatus one after another at the predetermined rate, each padded block being received serially, and wherein the apparatus further comprises:

means for outputting unpadded blocks at the predetermined rate.

27. The apparatus defined in claim 26 further comprising:

means for registering each successive padded block.

28. The apparatus defined in claim 27 wherein the means for registering is at least partly controlled by the first further clock signal.

29. The apparatus defined in claim 28 further comprising:

means for removing padding from each padded block registered by the means for registering to produce a corresponding unpadded block.

30. The apparatus defined in claim 29 further comprising:

means for converting each unpadded block to a plurality of successive sub-blocks.

31. The apparatus defined in claim 30 wherein the means for converting is at least partly controlled by the second further clock signal.

32. The apparatus defined in claim 25 wherein each padded block consists of 66 bits of data, and each unpadded block consists of 64 bits of data.

33. The apparatus defined claim 25 wherein the means for deriving comprises:

first frequency dividing circuitry for dividing frequency of a common signal by a first division factor to produce the second further clock signal, the common signal coming from the reference clock signal.

34. The apparatus defined in claim 33 wherein the means for deriving further comprises:

second frequency dividing circuitry for dividing the frequency of the common signal by a second division factor to produce the first further clock signal.

35. The apparatus defined in claim 33 wherein the means for deriving further comprises:

frequency multiplying circuitry for multiplying frequency of a signal coming from the reference clock signal to produce the common signal.

36. The apparatus defined in claim 35 wherein the means for deriving further comprises:

frequency pre-division circuitry for dividing frequency of the reference clock signal by a pre-division factor to produce the signal operated on by the frequency multiplying circuitry.

37. The apparatus defined in claim 26 wherein the reference clock signal has a reference frequency having an integer-based relationship to the predetermined rate.

38. The apparatus defined in claim 37 wherein the means for deriving comprises:

means for performing integer-based manipulation of the reference frequency to produce the first and second further clock signals.

39. The apparatus defined in claim 38 wherein the means for performing comprises:

first means for performing first integer-based manipulation of the reference frequency to produce a common signal; and

second means for performing second integer-based frequency manipulation of the common signal to produce the second further clock signal.

40. The apparatus defined in claim 39 wherein the means for performing further comprises:

third means for performing third integer-based frequency manipulation of the common signal to produce the first further clock signal.

41. The apparatus defined in claim 25 further comprising:

byte alignment circuitry for using the padding of the padded blocks to locate data block boundaries.

42. A method of padding and transmitting initially unpadded blocks of data comprising:

deriving from a reference clock signal a common signal;

producing first and second further clock signals from the common signal;

using the first further clock signal in at least some processing of the unpadded data; and

using the second further clock signal in at least some processing of the padded data, wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal.

43. The method defined in claim 42 wherein the common signal frequency is different from frequency of the reference signal.

44. The method defined in claim 42 wherein the first and second frequencies are both different from the common signal frequency.

45. The method defined in claim 42 wherein the deriving comprises:

using integer-based frequency manipulation of the reference clock signal to produce the common signal.

46. The method defined in claim 42 wherein the producing comprises:

using integer-based frequency manipulation of the common signal to produce at least one of the first and second further clock signals.

47. A method of receiving and unpadding padded blocks of data comprising:

deriving from a reference clock signal a common signal;

producing first and second further clock signals from the common signal;

using the first further clock signal in at least some processing of the padded data; and

using the second further clock signal in at least some processing of the unpadded data, wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal.

48. The method defined in claim 47 wherein the common signal frequency is different from frequency of the reference signal.

49. The method defined in claim 47 wherein the first and second frequencies are both different from the common signal frequency.

50. The method defined in claim 47 wherein the deriving comprises:

using integer-based frequency manipulation of the reference clock signal to produce the common signal.

51. The method defined in claim 47 wherein the producing comprises:

using integer-based frequency manipulation of the common signal to produce at least one of the first and second further clock signals.

52. Apparatus for padding and transmitting initially unpadded blocks of data comprising:

first circuitry adapted to derive from a reference clock signal a common signal;

second circuitry adapted to produce first and second further clock signals from the common signal;

third circuitry adapted to use the first further clock signal in at least some processing of the unpadded data; and

fourth circuitry adapted to use the second further clock signal in at least some processing of the padded data, wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal.

53. The apparatus defined in claim 52 wherein the common signal frequency is different from frequency of the reference clock signal.

54. The apparatus defined in claim 52 wherein the first and second frequencies are both different from the common signal frequency.

55. The apparatus defined in claim 52 wherein the first circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.

56. The apparatus defined in claim 55 wherein the second circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.

57. Apparatus for receiving and unpadding padded blocks of data comprising:

first circuitry adapted to derive from a reference clock signal a common signal;

second circuitry adapted to produce first and second further clock signals from the common signal;

third circuitry adapted to use the first further clock signal in at least some processing of the padded data; and

fourth circuitry adapted to use the second further clock signal in at least some processing of the unpadded data, wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal.

58. The apparatus defined in claim 57 wherein the common signal frequency is different from frequency of the reference clock signal.

59. The apparatus defined in claim 57 wherein the first and second frequencies are both different from the common signal frequency.

60. The apparatus defined in claim 57 wherein the first circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.

61. The apparatus defined in claim 60 wherein the second circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.